FIG. 1 (PRIOR ART)

I1(branch Loop)
I2
I3(Not in Cache Memory)

. .

Loop I10
I11
I12

FIG. 2A

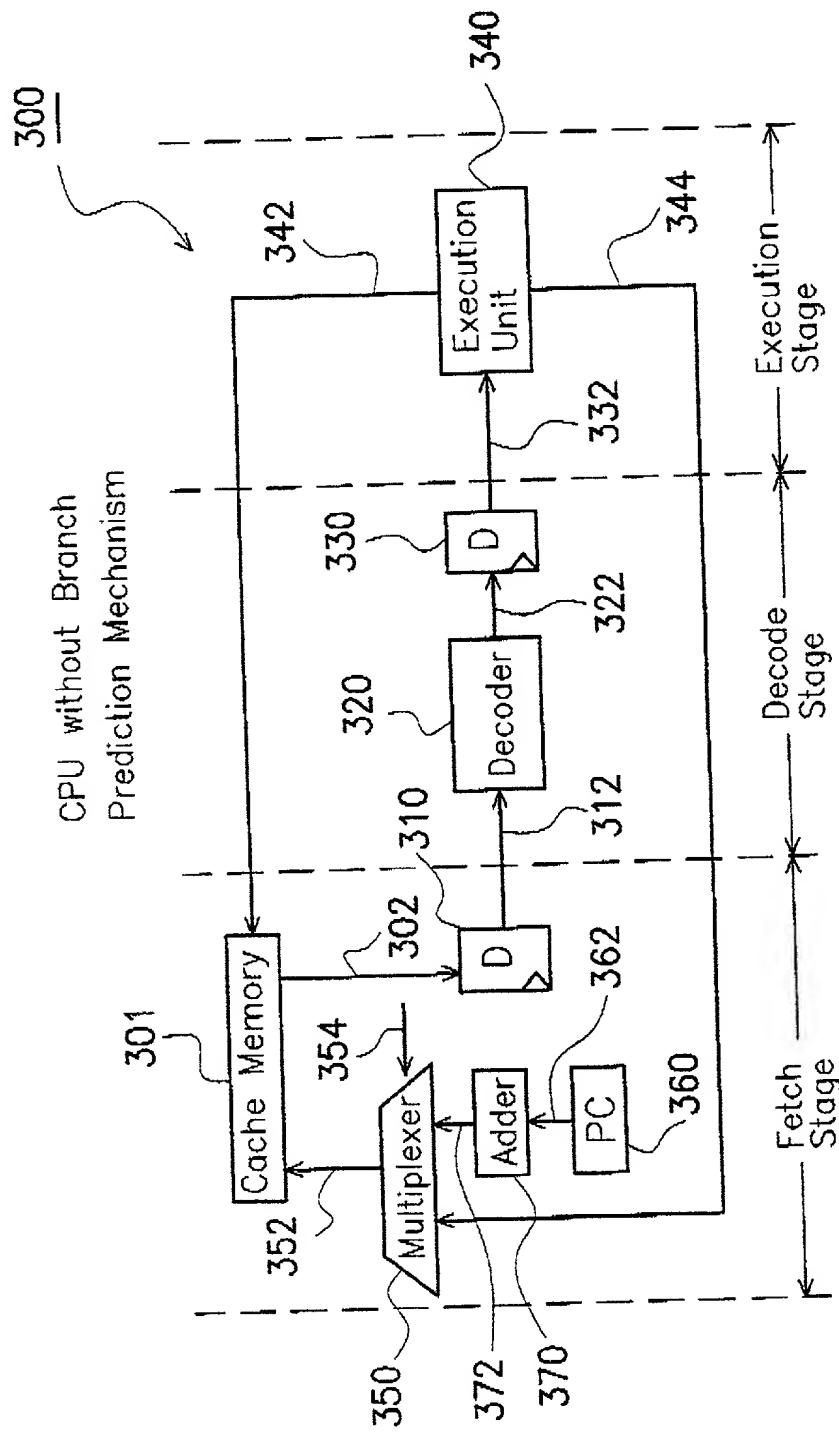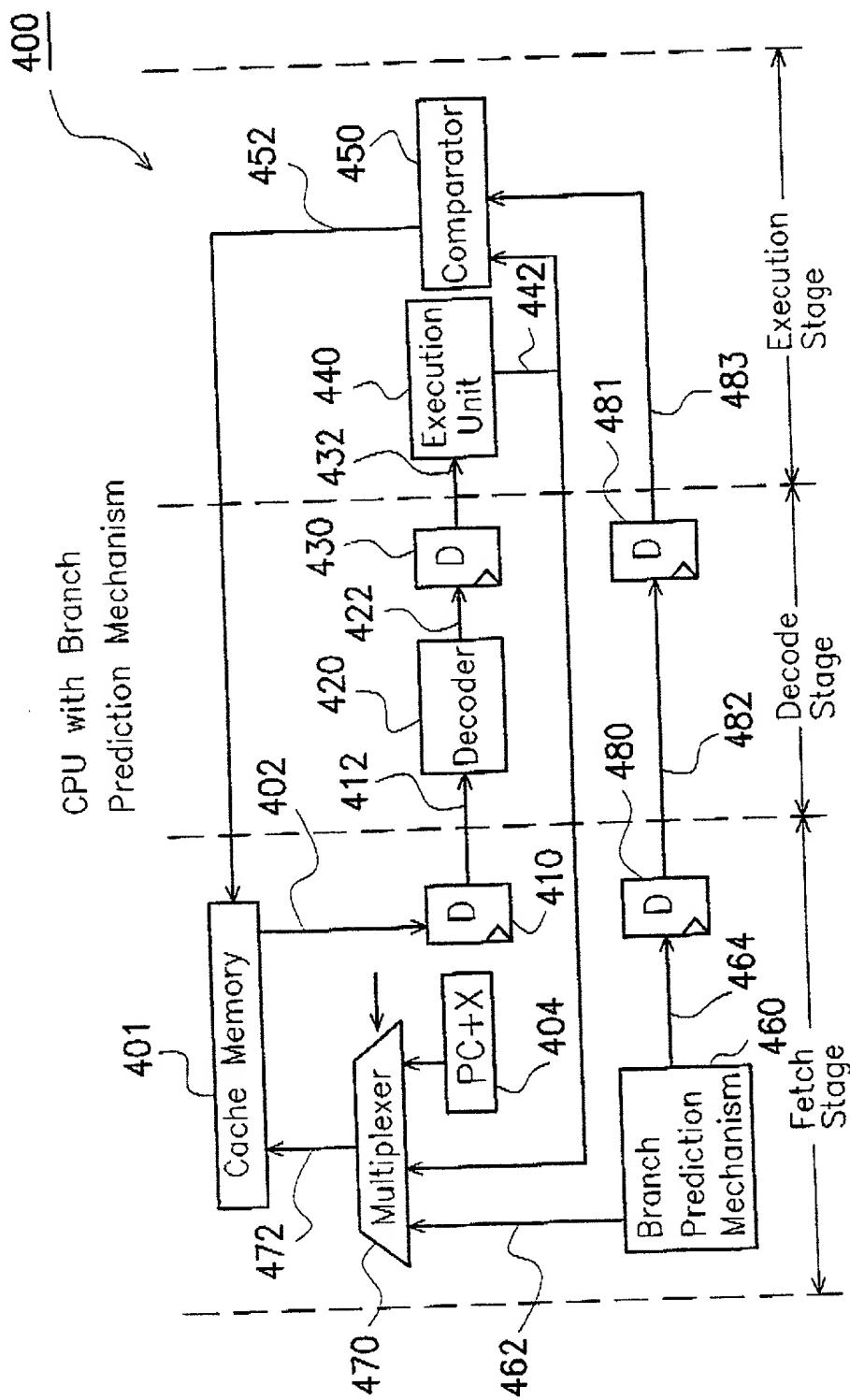|	C1	C2	C3	C4	C5	C6	C7	C8		
Fetch	I1	I2	I3	I3	I3	I10	I11	I12		
Decode		I1	I2	I2	I2	I2	I10	I11		
Execute			I1	I1	I1	I1	I2	I10		

FIG. 2B

CPU without Branch Prediction Mechanism

FIG. 3

CPU with Branch
Prediction Mechanism

FIG. 4

	C_1	C_2	C_3	C_4	C_5	C_6	
Fetch	I_1	I_2	I_3	I_{10}	I_{11}	I_{12}	
Decode		I_1	I_2	I_3	I_{10}	I_{11}	
Execute			I_1	I_2	I_3	I_{10}	

FIG. 5